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ATTN: BOX PATENT APPLICATION

OFGS File No. : IR-1677 (2-1984)
Inventor : Zhijun Qu and Kenneth Wagers
Title : DUAL EPITAXIAL LAYER FOR HIGH VOLTAGE CONDUCTION POWER MOSFET DEVICES
Assignee : International Rectifier Corporation

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

9 Pages of Specification including Abstract and Claims
12 Numbered Claims Calculated as 12 Claims for Fee Purposes
4 Sheets of Drawing Containing Figures 1 to 5.
X Declaration and Power of Attorney
_____ Priority is Claimed under 35 U.S.C. §119:
Convention Date _____ for _____ Appln. S.N. _____
X Assignment
_____ Information Disclosure Statement, PTO-1449 and references
X Return-Addressed Post Card
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DUAL EPITAXIAL LAYER FOR HIGH VOLTAGE VERTICAL CONDUCTION POWER MOSFET DEVICES

FIELD OF THE INVENTION

This invention relates to MOSFET semiconductor devices and more specifically relates to a novel structure and process for manufacture of a vertical conduction power MOSFET device which has a reduced on resistance.

BACKGROUND OF THE INVENTION

Vertical conduction Power MOSFET devices are well known. Such devices may be made as disclosed, for example, in U.S. Patent 5,007,725, as planar, cellular devices, or can be made with a well known parallel stripe topology, or can be made using a trench technology.

The on-resistance (RDSON) of such devices is dependant in large measure on the resistivity of the epitaxially formed silicon layer which receives the device junctions, and this resistivity is, in turn, determined by the blocking voltage requirement of the final device. Thus, higher blocking voltages require a higher resistivity in the epitaxial layer, but this then causes an increase on resistance for the device.

It would be very desirable to provide a structure for high voltage devices, particularly those having a blocking voltage greater than about 100 volts, which can have a reduced on-resistance without sacrificing any substantial blocking voltage.

BRIEF DESCRIPTION OF THE INVENTION

A novel dual (or graded) epitaxial junction-receiving layer is provided in accordance with the invention in which two layers are sequentially epitaxially deposited atop a silicon substrate. The lower layer has a uniform resistivity which is higher than that of the uniform resistivity of the upper layer. The upper layer has a depth sufficiently thick to receive all device junctions and may be about one fifth of the thickness of the lower layer. Furthermore, it has been found possible to reduce the total thickness of the two epi layers from that which was necessary for a single layer epi of the prior art, as will be later described, thereby producing a reduced on-resistance for a given design rating.

It has been found that the novel structure of the invention will produce a reduction in on-resistance of a given device design by greater than about 10% in exchange for no reduction in breakdown voltage.

BRIEF DESCRIPTION OF THE DRAWING(S)

Figure 1 is a cross-sectional view of a typical prior art vertical conduction MOSFET with a single junction receiving epitaxial layer.

Figure 2 is a diagram showing the electric field in the single epi layer of Figure 1 as a function of depth during a voltage blocking condition.

Figure 3 is a cross-sectional view of the dual epitaxial layer structure used in accordance with the invention.

Figure 4 shows a diagram like that of Figure 2, but modified in accordance with the invention.

Figure 5 shows a bar graph comparison of a single layer epi structure and the rating-equivalent dual layer epi structure of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring first to Figure 1, there is shown a typical vertical conduction MOSFET in cross-section as having a highly conductive N^{++} substrate 10 which has a single epitaxially deposited N^- layer 11 thereon. N^- layer 11 receives the various junctions needed to create the device such as spaced P type base diffusions 12 and 13 which contain N^+ source diffusion rings 14 and 15 respectively (for a cellular topology).

The invertible channel areas between the peripheries of the source rings and base diffusions are covered with a gate oxide layer 16 and a conductive polysilicon gate electrode 17. Gate electrode 17 is covered by an interlayer oxide 18 and the device upper surface is covered by an aluminum source electrode 19. The bottom of the wafer or chip receives a drain electrode 20.

The structure of Figure 1 is typical of many kinds of devices which can benefit from the invention, as will be later described. Thus, the device, shown as an N channel device, can be a P channel device (reversing all conductivity types) and the device can employ a trench topography instead of the planar topography shown.

In designing the device of Figure 1, two key design parameters are reverse blocking voltage and on resistance. The device blocking voltage is function of the thickness of epi layer 11 and its resistivity ρ. More specifically, if the electric field in the epi layer 11 is plotted against depth, as in Figure 2, the blocking

voltage can be shown to be proportional to the shaded area under the curve. The device on-resistance is proportional to the resistivity ρ of the epi and is inverse proportional to the slope of the straight line in Figure 2. It will be seen that if blocking voltage is increased, the slope of the curve must decrease. Thus, design trade-offs are always need for designing a device with a given blocking voltage or given on-resistance.

The present invention permits the designer to change the shape of the curve of Figure 2 in such a way that the area (blocking voltage) can be increased (or kept about constant) while the total epi depth can be reduced and the slope of the line can be generally unchanged for the bulk of the epi depth. More specifically, and as shown in Figure 3, the epi layer 11 of Figure 1 is divided into an upper junction receiving layer of reduced resistivity and a lower epi layer 21 of greater resistivity than that of layer 20, but of greater thickness. In a 600 volt device layer 20 of Figure 3, typically may be about 10 microns thick, and greater than the depth of the base junctions 12 and 13. Layer 21 is thicker than layer 20 for high voltage device. Obviously different values will be used for different breakdown voltages. In general, the resistivity of lower layer 21 is higher than that of layer 20.

For a conventional 600 volt device, epi layer 11 of Figure 1 is typically 21.5 ohm-cm and 57 microns thick. This produces a device with on-resistance of about 0.68 ohms. This device is replaced, in accordance with the invention, by the device of Figure 3 in which layer 20 is 7 ohm-cm (a value which would be used for a 250 volt device) while layer 21 is 21.5 ohm-cm material

(conventional for 600 volt devices). Layers 20 and 21 have thicknesses of 7 and 48 microns respectively.

The effect of this dual layer structure, with a lower resistivity upper layer 20 is shown in Figure 4. The line 30 in Figure 4 has the same slope as the line in Figure 2. However, the area under the curve of Figure 4 is increased by the shaded area 31 caused by the segment 32 of greater slope. Thus, in Figure 4, the lower resistivity epi 20 of Figure 3 has the depth x_i; and the total depth of regions 20 and 21 is reduced from depth W (for the design of Figure 1) to W'.

Consequently, the device of Figure 3 has the same breakdown voltage as that of Figure 2 since the area under the curve in Figure 4 is about the same as that of Figure 2. However, the on-resistance is reduced because of the total reduced epi depth and the reduced resistivity in the first epi layer. These resistance comparisons are listed directly on Figure 4, comparing the total on-resistances of the single and dual epi layer embodiments.

Figure 5 shows the breakdown voltage and on-resistances of equivalent devices using single and dual epi structures.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising, in combination, a silicon substrate having a first and second surface; a first epitaxially deposited layer formed atop said first surface and having impurities of the n or p conductivity type uniformly distributed throughout the volume of said first layer; a second epitaxially deposited layer deposited atop the surface of said first layer and having impurities of the same type as those in said first layer uniformly distributed therethrough; the concentration of impurities in said second layer being greater than the concentration of impurities in said first layer; and a plurality of diffusions of a conductivity type opposite to that of said second layer uniformly distributed into the surface of said second layer and defining p-n junctions therein.

2. The device of claim 1 wherein the resistivity of said second layer is higher than that of said first layer.

3. The device of claim 1 wherein the thickness of said first layer is more than that of said second layer.

4. The device of claim 2 wherein the thickness of said first layer is more than that of said second layer.

5. The device of claim 1 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.

6. The device of claim 2 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.

7. The device of claim 3 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.

8. The device of claim 4 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.

9. The device of claim 8 wherein said device is a vertical conduction power MOSFET.

10. A vertical conduction power MOSFET device having a reduced on-resistance; said device comprising a silicon substrate having a drain electrode on the bottom surface thereof, and an epitaxially deposited layer on the upper surface of said substrate; said epitaxial deposited layer having a graded concentration of one of the conductivity types from its top free surface to its bottom; an upper portion of said epitaxial layer extending from its free surface receiving a P-N junction which at least partly defines said power MOSFET and having an average impurity concentration which is more than the average concentration of the bottom portion of said epitaxial layer; said bottom portion of said epitaxial layer comprising more than 50% of the total thickness of said epitaxial layer.

11. The device of claim 10 wherein said lower and upper portions of said epitaxial layer comprise respective separately deposited first and second layers of respective uniform concentration or the upper portion of uniform doped epitaxial layer receives extra same type ion implantation and drive process.

12. The device of claim 11 wherein the total thickness of said first and second layers is less than the thickness of a single epitaxial layer designed to block the same voltage.

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DUAL EPITAXIAL LAYER FOR HIGH VOLTAGE VERTICAL CONDUCTION POWER MOSFET DEVICES

ABSTRACT OF THE DISCLOSURE

The epitaxial silicon junction receiving layer of a power semiconductor device is formed of upper and lower layers. The lower layer has a resistivity of more than that of the upper layer and a thickness of more than that of the upper layer. The total thickness of the two layers is less than that of a single epitaxial layer that would be used for the same blocking voltage. P-N junctions are formed in the upper layer to define a vertical conduction power MOSFET device. The on-resistance is reduced more than 10% without any blocking voltage reduce. The upper epitaxial layer can be either by direct second layer deposition or by ion implantation of a uniform epitaxial layer followed by a driving process.

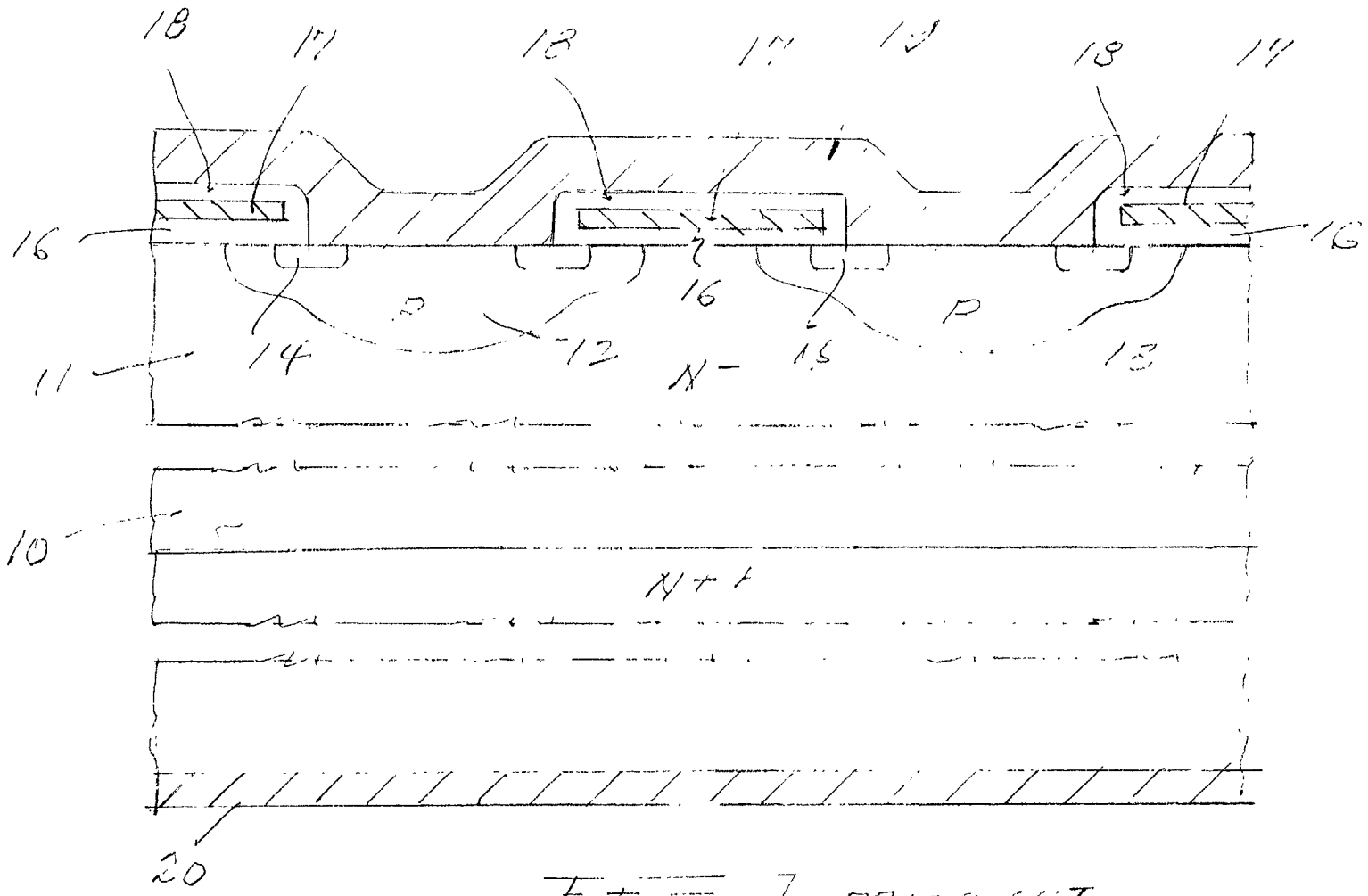


FIG. 1 PRIOR ART

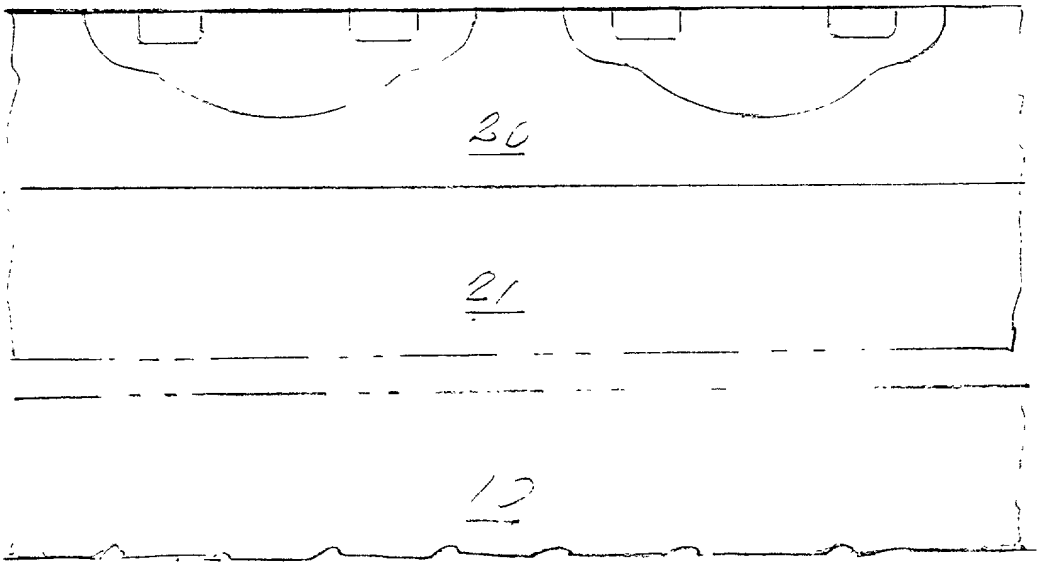


FIG. 3

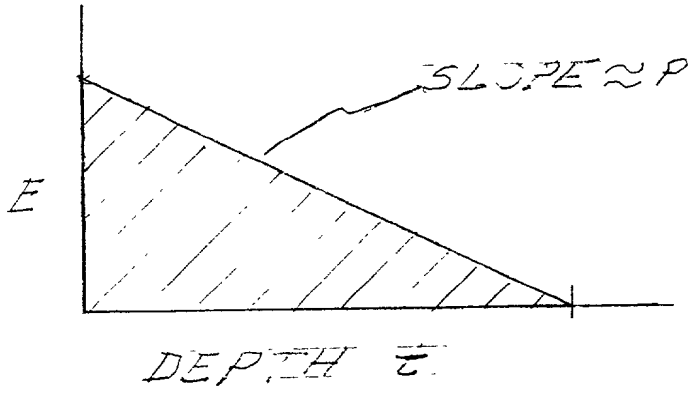
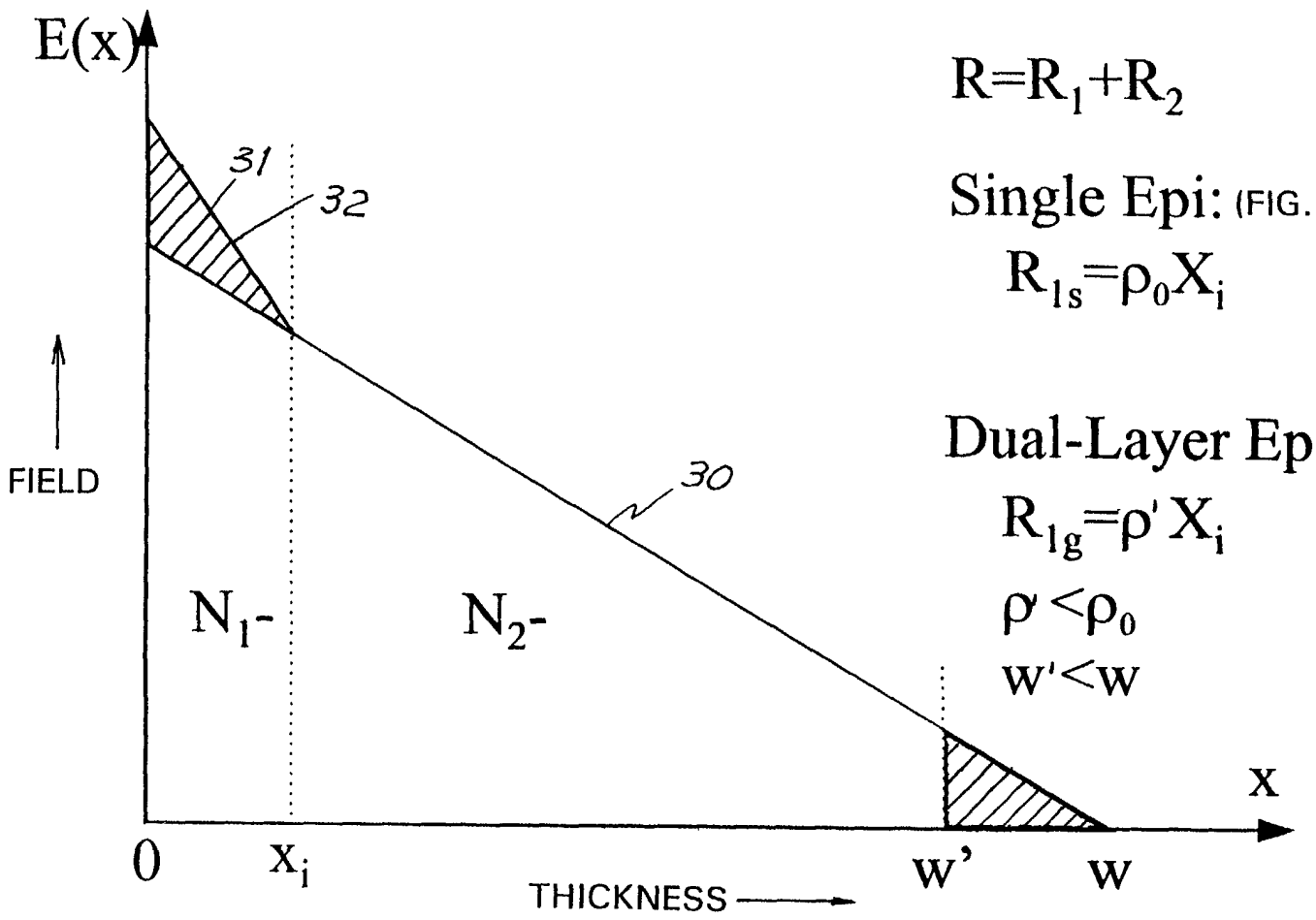


FIG. 2



$R=R_1+R_2$

Single Epi: (FIG. 1)

$R_{1s}=\rho_0 X_i$ $R_{2s}=\rho_0(w-X_i)$

Dual-Layer Epi (FIG. 3)

$R_{1g}=\rho' X_i$ $R_{2g}=\rho_0(w'-X_i)$

$\rho' < \rho_0$ $R_{1g} < R_{1s}$

$w' < w$ $R_{2g} < R_{2s}$

FIG. 4

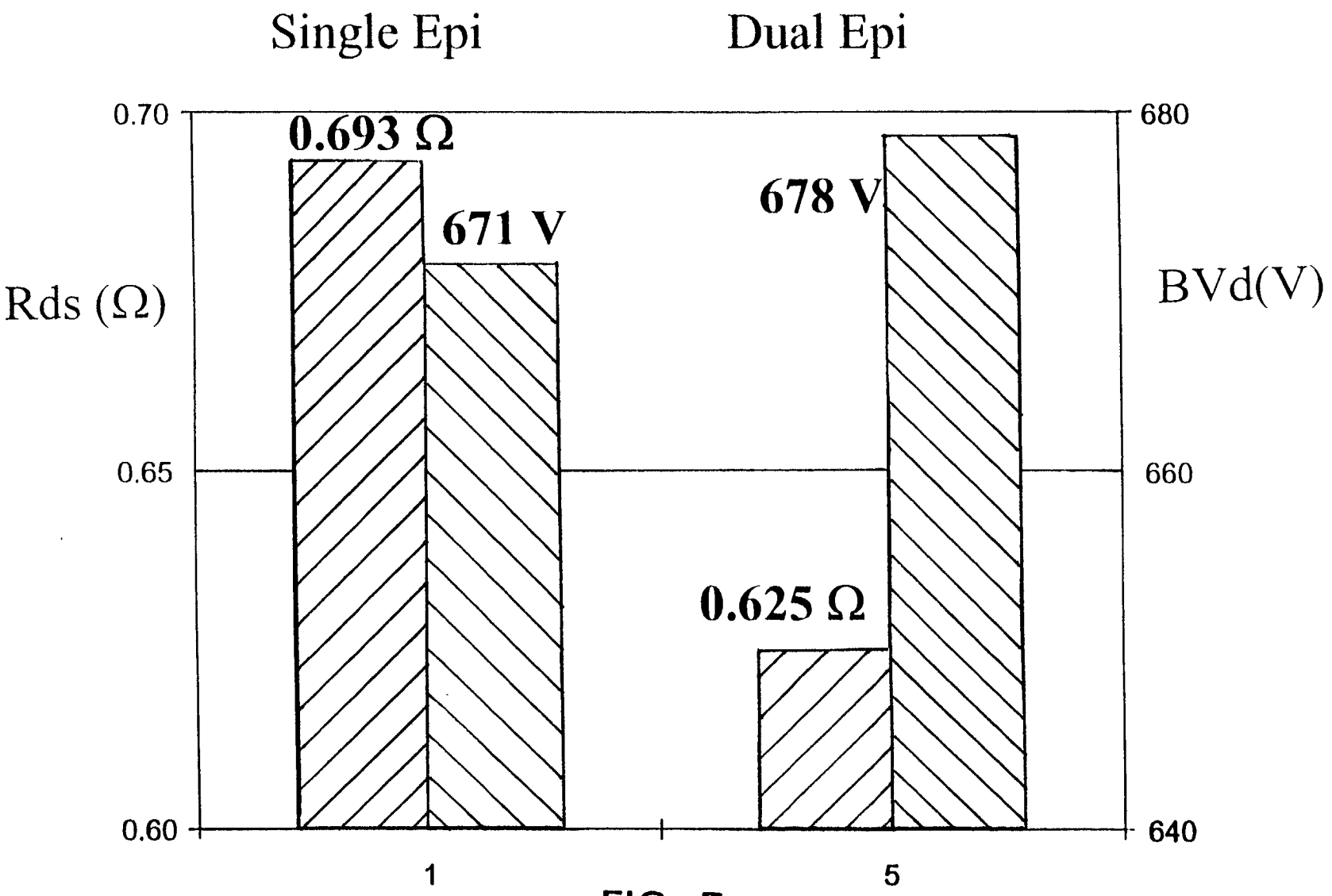


FIG. 5

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As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DUAL EPITAXIAL LAYER FOR HIGH VOLTAGE VERTICAL CONDUCTION POWER MOSFET DEVICES

the specification of which is attached hereto, unless the following box is checked:

☐ was filed on _____ as United States patent Application Number or PCT International patent application number _____ and was amended on _____ (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign or Provisional Application(s)

COUNTRY	APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES ____ NO ____
			YES ____ NO ____
			YES ____ NO ____

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

UNITED STATES APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	STATUS *(patented, pending, abandoned)*

I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB & SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944; Louis C. Dujmich - Reg. No. 30,625 and Douglas A. Miro - Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.

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